朝陽科技大學 098學年度第2學期教學大綱
Introduction to Digital Integrated Circuit Design 數位積體電路設計概論

當期課號	3868	Course Number	3868
授課教師	張原豪	Instructor	CHANG,YUEN HAW
中文課名	數位積體電路設計概論	Course Name	Introduction to Digital Integrated Circuit Design
開課單位	資訊工程系(四進)四A	Department	
修習別	選修	Required/Elective	Elective
學分數	3	Credits	3
課程目標	.本課程在介紹使用電腦輔助工具及硬體描述語言來進行數位積體電路或系統的設計. 2.內容:架構層/行爲層概念, Verilog硬體描述語言,行爲層/暫存器層/閘層設計,FPGA實現與工具,平面化置放與佈線過程,MOS反相器靜態/動態特性,靜態邏輯電路:組合電路設計,靜態邏輯電路:序向電路設計,動態邏輯電路設計,半導體記憶體,晶片輸出入電路,專題研究.	Objectives	1.This course presents the design of digital integrated circuits via FPGA CAD tool and Vrilog code. 2. Content: Architecture/Behavior Concepts, Verilog HDL Programming, Behavior/RTL/Gate-level Design, FPGA Implementation and Tools, Floor plan, Placement & Route, MOS Inverters: Static/Dynamic Characteristics, Static Logic Circuits: Combinational, Static Logic Circuits: Sequential, Dynamical Logic Circuits, Semiconductor Memories, Chip Input and Output Circuits, Case Study.
教材	1. Verilog HDL, Samir Palnitkar (Sun 2003). 2. Vrilog Styles for Synthesis of Digital Systems, David R. Smith, Paul D. Franzon (Prentce-Hall,2000) 3. Veilog硬體描述語言數位電路, 鄭信源, 儒林圖書, 2003. 4. CMOS Digital Integrated Circuits –analysis & design, S-M. Kang, Y. Leblebici (McGraw-Hill, 2002).	Teaching Materials	1. Verilog HDL, Samir Palnitkar (Sun 2003). 2. Vrilog Styles for Synthesis of Digital Systems, David R. Smith, Paul D. Franzon (Prentce-Hall,2000) 3. Veilog硬體描述語言數位電路, 鄭信源, 儒林圖書, 2003. 4. CMOS Digital Integrated Circuits –analysis & design, S-M. Kang, Y. Leblebici (McGraw-Hill, 2002).
成績評量方式	1. 40% 期中/期末考 2. 20% 作業 3. 20% 期末作業 4. 平時20%(出席)	Grading	1. 40% Middle/Final exam. 2. 20% Homework 3. 20% Final project 4. Learning attitute: 20%
教師網頁	_		
教學內容	1. 架構層/行爲層概念 2. Verilog硬體描述語言 3. 階層式模組設計 4. 行爲層/暫存器層/閘層設計 5. FPGA實現 6. 平面化過程 7. 置放與佈線 8. 佈局過程 9. 專題實作研究 4. CMOS Digital Integrated Circuits –analysis & design, S-M. Kang, Y. Leblebici (McGraw-Hill, 2002).	Syllabus	1. Architecture/Behavior Concepts 2. Verilog HDL Programming 3. Hierarchical Modeling 4. Behavior/RTL/Gate-level Design 5. FPGA Implementation 6. Floor plan 7. Placement & Route 8. Layout 9. Case Study