朝陽科技大學 098學年度第2學期教學大綱
Digital Logic Design 數位邏輯設計

當期課號	2872	Course Number	2872
授課教師	魏清泉	Instructor	WEI,CHING CHUAN
中文課名	數位邏輯設計	Course Name	Digital Logic Design
開課單位	資訊與通訊系(四日)一A	Department	
修習別	必修	Required/Elective	Required
學分數	3	Credits	3
課程目標	"本課程的目標有 1. 使學生了解進制演算、邏輯閘、加法器與減法器、編碼與多工、正反器、序向邏輯及其應用(知識) 2.使學生了解並熟悉布林代數之運算，以達成邏輯運算之簡化，並降低邏輯閘的數目(能力) 3. 使學生知道邏輯運算及其網路應用之重要性(態度) 4. 使學生了解暫存器、計數器、記憶體及可程式邏輯與其在微處理器之應用及網路應用 (其他)"	Objectives	"The goals of this course are described as follows. 1. Enable students to understand the binary operations, logic gates, the Adder and Subtractor, coding and multiplexer, Flip-Flops and the applications, the sequential logic and the microprocessors applications. 2. Enable students to learn and to become familiar with the operation of Boolean algebra, with logical operations of simplification, and reduce the number of logic gates. 3. Make the students know that the logic design and its applications are important for the computer engineering and network applications. 4. Make the students understand registers, counters, the memory, the programable logic and its application in the microprocessors. "
教材	教科書：Digital Design, Mano, 4/e 滄海書局 參考書：Digital Electronics Principles & Applications, 6th ed, Roger L. Tokheim, McGraw-Hill	Teaching Materials	Textbook：Digital Design, Mano, 4/e Reference：Digital Electronics Principles & Applications, 6th ed, Roger L. Tokheim, McGraw-Hill
成績評量方式	1. 期中考: 30% 2. 期末考30% 3. 其他: 40% (含學習態度、作業、小考、報告)	Grading	1. Midterm exam. : 30% 2. Final exam. :30% 3. Others(learning attitude, homework, quiz, report..): 40%
教師網頁	http://www.cyut.edu.tw/~chcheng		
教學內容	1. 數字系統轉換與布林代數 2. 布林代數表示與化簡 3. 基本邏輯閘介紹 4. NAND/NOR多階組合數位電路 5. 加法器,多/解多工器,解/編碼器之介紹 6. 組合邏輯設計 7. 正反器與激勵表 8. 狀態圖及狀態激勵表 9. 同步計數器設計 10. 狀態表簡化 11. 遞迴網路設計 12. MSI序向網路設計 13. ROM/PLA/PAL序向網路設計 14. 算術網路設計	Syllabus	1. Number system and Boolean algebra 2. Boolean algebra 3. Introduction to basic logic gates 4. NAND/NOR muulti-level digital circuit 5. Adder, multiplex/demultiplex, decoder/encoder 6. Combinational logic design 7. Flip-flop and exciting table 8. State diagram and state exciting table 9. Synchronous counter design 10. State table reduction 11. Recursive network design 12. MSI sequential network design 13. ROM/PLA/PAL sequential network design 14. ALU network design

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