朝陽科技大學 097學年度第1學期教學大綱
Digital Systems 數位系統

當期課號	2660	Course Number	2660
授課教師	劉省宏	Instructor	LIU,SHING HONG
中文課名	數位系統	Course Name	Digital Systems
開課單位	資訊工程系(四日)一B	Department	
修習別	必修	Required/Elective	Required
學分數	3	Credits	3
課程目標	這個課程介紹數位系統設計與實務，內容包含邏輯電路的基本觀念、電子電路實作邏輯電路、邏輯函數的最佳化、以較大型組合電路來設計邏輯函數、儲存元件、同步與非同步序向電路。在基本觀念上，說明布林代數與邏輯閘；在電子電路實作與邏輯函數最佳化的課程中，我們使用CAD工具來設計與合成電路；接著介紹利用解碼器、編碼器、與多工器來設計邏輯函數；序向電路是另一個重點，包括：位移記錄器、計數器、有限狀態機、以及CAD工具。	Objectives	This course is an introduction to the design and implementation of digital systems. We will study various topics including basic aspects and electronic aspects of logic circuits, optimized implementation of logic functions, combinational circuits used as building blocks, storage elements, synchronous and asynchronous sequential circuits. In the basic aspects of logic circuits, we will study Boolean algebra, logic gates; in the electronic aspects and optimized implementation of logic functions, we study how to synthesize combinational circuits using logic gates and CAD tools. Using decoder, encoders, and multiplexers as building blocks in larger design is presented. Following the studies of combinational circuits, sequential circuits are introduced. We study the storage element (flip-flops), realization of shift registers and counters; explain the behavior of synchronous (asynchronous) sequential circuits (finite state machines) and develop practical design technique for both manual and automated design.
教材	1. 教科書 "Digital Design" 滄海書局 2. 使用黑板和簡報教授課程 3. 指定作業練習和平實考 4. 實施期中和期末考	Teaching Materials	1. Text book. "Digital Design" 2. speak teaching by board and PPT 3. Home work and test 4. Midtern and final exam.
成績評量方式	1. 期中和期末各30% 2. 小考和作業外加出席率40%	Grading	1. Midterm/ final exam: 30% respectively. 2. Home work, test, and learning attitute 40%
教師網頁			
教學內容	數字系統, 布林函數, 坎諾圖, 組合邏輯電路設計, 基本邏輯元件介紹, 正反器, 暫存器, 計數器, 狀態圖與狀態分配, 序相邏輯電路設計, VHDL語言簡介	Syllabus	Number Systems, Boolean Algebra, Karnaugh Maps, Combinational Circuit Design, Basic Logic Devices, Latch and Flip-Flops, Registers and Counters, State table and State Assignment, Clocked Sequential Circuit Design, Introduction to VHDL

尊重智慧財產權，請勿非法影印。