朝陽科技大學 093學年度第1學期教學大綱
Special Topic on Signal Processing（Ⅰ）訊號處理專題(一)

當期課號	7792	Course Number	7792
授課教師	張原豪	Instructor	CHANG,YUEN HAW
中文課名	訊號處理專題(一)	Course Name	Special Topic on Signal Processing (Ⅰ)
開課單位	資訊工程系碩士在職專班一A	Department	
修習別	選修	Required/Elective	Elective
學分數	2	Credits	2
課程目標	本課程爲實務課程，授課內容主要爲將學生所學有關訊號處理的知識實際應用於語音及影像處理上。課程內容將講授包括-類比訊號、離散訊號、類比系統以及離散系統的時域表示法和頻域表示法。學生在完成本課程後，將可利用以下之基本原理：1. 內積和運算、2.傅立葉轉換、3. 取樣原理、4. 數位濾波器原理等進行語音及影像處理。	Objectives	The goal of this course is to teach the students to implement the signal processing on image processing with speech processing. In this course the students will learn include the time domain and frequency domain of analog signal、discrete signal、analog system and discrete system. The students will realize the following basics after finishing this course: 1. the convolution theory, 2. the Fourier transform, 3. the sampling theory, 4. the application of digital filter theory. Finally, the students will use above knowledges to implement on image processing and speech processing.
教材	1.handout 2.papers	Teaching Materials	
成績評量方式	project 60% homework 40%	Grading	project 60% homework 40%
教師網頁			
教學內容	本課程配合CIC之Cell-Based Design Flow，介紹邏輯電路合成的基本知識及如何用HDL撰寫有效率可合成之電路，並以Synopsys爲工具，配合Avant! 0.35um Cell Library 導引學員如何將自己的Verilog或VHDL設計，根據電路環境條件及所需之速度、面積及功率，進行電路合成最佳化,達成DSP演算晶片化之設計工作.	Syllabus	1.Introduction of Logic Synthesis -- Design object -- Static Timing Analysis (STA) -- Synopsys design analyzer environment 2.HDL Coding for Synthesis -- Synthesizable verilog HDL -- Some tricks in verilog HDL -- Designware library -- Partition for synthesis 3. Design Constraint -- Setting design environemnt -- Setting design constraint 4. Design Optimization -- Compile the design -- Finite state machine optimization 5. Synthesis Report and Analysis

尊重智慧財產權，請勿非法影印。